Low-Volume & MPW Service

IHP offers research partners and customers access to its powerful SiGe:C BiCMOS technologies and special integrated RF modules.
These technologies are especially suited for applications in the higher GHz bands (e.g. for wireless, broadband, radar). They provide integrated HBTs with cut-off frequencies of up to 500 GHz and integrated LDMOS devices with breakdown voltages of up to 22 V, including complementary devices.

SiGe:C BiCMOS Technologies for MPW & Prototyping

SG25H3: A 0.25 µm technology with a set of npn-HBTs ranging from a higher RF performance (f_T/f_{ma}x = 110/180 GHz) to higher breakdown voltages up to 7 V.

SG25H4: A high performance BiCMOS technology. Process is identical to former SG25H1 technology, only Process Design Kit is new. The bipolar module is based on H1 SiGe:C npn HBT's with up to 190 GHz transient frequencies and up to 220 GHz oscillation frequencies.

SGB25V: A cost-effective technology with a set of npn-HBTs up to a breakdown voltage of 7 V.

SG13S: A high-performance 0.13 µm BiCMOS with npn-HBTs up to f_T/f_{max} = 250/300 GHz, with 3.3 V I/O CMOS and 1.2 V logic CMOS.

SG13G2: A 0.13 µm BiCMOS technologies with same device portfolio as SG13S but much higher bipolar performance with f_T/f_{max} = 300/500 GHz

The backend offers 3 (SG13: 5) thin and 2 thick metal layers (TM1: 2 µm TM2: 3 µm)

The schedule for MPW & Prototyping runs is located at
www.ihp-microelectronics.com

Cadence-based mixed signal Design Kit is available. For high frequency designs an analog Design Kit in ADS can be used. IHP's reusable blocks and IPs for wireless and broadband are offered to support your designs.

The following Modules are available

GD: Additional integrated complementary RF LDMOS devices with nLDMOS up to 22 V, pLDMOS up to -16 V breakdown voltage and an isolated nLDMOS device (available in SGB25V).

H3P: Additional pnp-HBTs with f_T/f_{max} = 90/120 GHz for complementary bipolar applications (available in SG25H3)

RFMEMS Module is an additional option in SG13S and SG13G2 technologies which offers integrated capacitive RFMEMS switch devices for frequencies between 40 GHz to 150 GHz.

LBE The Localized Backside Etching module is offered to remove silicon locally to improve passive performance (available in all technologies).

PIC Additional photonic design layers together with BiCMOS BEOL layers on SOI wafers (available in SG25H1/H3)

Bipolar Section

SG25H3	High Perf.	Medium Volt.	High Volt.	PNP module
A_E	0.22 x 0.84	0.22 x 2.24	0.22 x 2.24	0.22 x 0.84
Peak f_{max}	180 GHz	140 GHz	80 GHz	120 GHz
Peak f_T	110 GHz	45 GHz	25 GHz	90 GHz
BV_{CEO}	2.3 V	5 V	> 7 V	-2.5 V
BV_{CBO}	6.0 V	15.5 V	21.0 V	-4.0 V
V_A	30 V	30 V	30 V	30 V
β	150	150	150	100

SG25H4	npn1	npn2	Medium Volt.	High Volt.
A_E	0.21 x 0.84	0.18 x 0.84	0.22 x 2.24	0.22 x 2.24
Peak f_{max}	190 GHz	220 GHz	140 GHz	80 GHz
Peak f_T	190 GHz	200 GHz	45 GHz	25 GHz
BV_{CEO}	1.9 V	1.9 V	5 V	> 7 V
BV_{CBO}	4.5 V	5.0 V	15.5 V	21.0 V
V_A	40 V	40 V	30 V	30 V
β	270	260	150	150

SGB25V	High Perf.	Standard	High Volt.
A_E	0.42 x 0.84	0.42 x 0.84	0.42 x 0.84
Peak f_{max}	95 GHz	90 GHz	70 GHz
Peak f_T	75 GHz	45 GHz	25 GHz
BV_{CEO}	2.4 V	4.0 V	7.0 V
BV_{CBO}	> 7 V	> 15 V	> 20 V
V_A	> 50 V	> 80 V	> 100 V
β	190	190	190

SG13S	npn13P	npn13V
A_E	0.12 x 0.48	0.18 x 1.02
Peak f_{max}	340 GHz	165 GHz
Peak f_T	250 GHz	45 GHz
BV_{CEO}	1.7 V	3.7 V
BV_{CBO}	5.0 V	15 V
β	900	900

SG13G2	npn13G2
A_E	0.07 x 0.90
Peak f_{max}	500 GHz
Peak f_T	300 GHz
BV_{CEO}	1.7 V
BV_{CBO}	4.8 V
β	650

CMOS Section

		SG25H3/H4*	SG13S***	
Core Supply Voltage		2.5 V	3.3 V	1.2 V
nMOS	V_{TH}	0.6 V	0.71 V	0.50 V
	I_{OUT}**	540 µA/µm	280 µA/µm	480 µA/µm
	I_{OFF}	3 pA/µm	10 pA/µm	500 pA/µm
pMOS	V_{TH}	-0.6 V	-0.61 V	-0.47 V
	I_{OUT}	-230 µA/µm	-220 µA/µm	-200 µA/µm
	I_{OFF}	-3 pA/µm	-10 pA/µm	-500 pA/µm

* Parameters for SGB25V are similar ** @ V_G = 2.5 V
*** Parameters for SG13G2 have to be defined

Passive Section

	SG25H3/H4	SGB25V	SG13S
MIM Capacitor	1 fF/µm²	1 fF/µm²	1.5 fF/µm²
N^+ Poly Resistor	210 Ω/□	210 Ω/□	-
P^+ Poly Resistor	280 Ω/□	310 Ω/□	250 Ω/□
High Poly Resistor	1600 Ω/□	2000 Ω/□	1300 Ω/□
Varactor C_{max}/C_{min}	3	tbd.	tbd.
Inductor Q@ 5 GHz	18 (1 nH)	18 (1 nH)	18 (1 nH)
Inductor Q@10 GHz	20 (1 nH)	20 (1 nH)	20 (1 nH)
Inductor Q @ 5 GHz	37 (1 nH)*	37 (1 nH)*	37 (1 nH)*

* with LBE

GD-Module

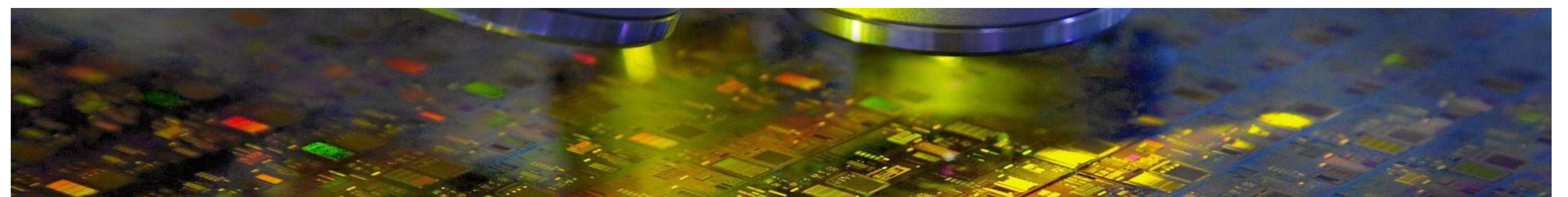
	n-LDMOS		p-LDMOS
	NLD2GD22C	iNLD2GD13A**	PLD2G19B
BV_{DSS}*	22 V	14 V	-16 V
V_{TH}	0.55 V	0.6 V	-0.5 V
I_{OUT}**	460 µA/µm	440 µA/µm	-180 µA/µm
R_{ON}	4 Ωmm	4 Ωmm	15 Ωmm
Peak f_{max}***	52 GHz	50 GHz	30 GHz
Peak f_t ***	20 GHz	28 GHz	9 GHz

* @ 50 pA/µm ** @ V_G = 2.5 V *** @ V_{DS} = 4 V
**** substrate isolated

RF MEMS Switch module

Actuation voltage	60 V (Pull-In ~50 V)
C_{on} / C_{off}	> 10
Switch time	< 10 µs
Isolation*	< 20 dB
Insertion loss*	< 1 dB

* @ 60 GHz



Photonic Integrated Circuit module

- 2 dopings (p+, n+)
- Full backend metal stack (3x metal + 2x top metal)
- Localized backside etching (optional)

Etch depth	220 nm	120 nm	70 nm
Waveguide loss	3.5 dB/cm (Waveguide width = 450 nm)	3 dB/cm (Waveguide width = 500 nm)	1 dB/cm (Waveguide width = 700 nm)
Smallest feature size	width>180 nm, notch/space>180 nm (remaining area is drawn)	width>180 nm, notch/space>400 nm (area being etched is drawn	width>130 nm, notch/space>30 nm (area being etched is drawn)

Germanium Photo Diode Building Block	Mach-Zehnder Modulator Building Block
Waveguide stub Bandwidth = 60 GHz @Bias = -2 V Responsivity = 0.9 A/W @ Bias= -2 V GDSII cell	5mm phase shifter length Designed for push-pull operation Bandwidth ~ 15 GHz Travelling Wave Electrode Design Insertion loss (including coupling) ~ 14 dB $V\pi$ ~ 6 V GDSII cell

Design Kit

The design kits support a Cadence mixed signal platform:

Analog/Mixed-Signal Flow:

- Design Framework II (Cadence 6.1)
- Schematic Design Entry (Cadence Virtuoso Schematic Editor)
- Simulation
  · Simulation Cockpit: Analog Design Environment – ADE (Cadence)
  · RF: SpectreRF (Cadence)
  · Analog: Spectre/APS (Cadence)
  · Mixed-Signal: AMS Designer/XPS (Cadence)
- Full Custom Layout (Cadence Virtuoso Layout Editor)
- Physical Verification (Cadence Assura: DRC/LVS, Cadence QRC: Parasitic Extraction, selected PDKs support Substrate Noise Analysis)
- Selected PDKs support Cadence VPS for EMIR analysis
- Support of Analog Office and TexEDA via partners is available
- Sonnet support for all design kits
- ADS-support via Golden Gate/RFIC dynamic link to Cadence is available
- Standalone ADS Kit including Momentum substrate layer file

Digital Design Flow:

- Behavioral Modeling (VHDL, Verilog HDL)
- Verification
  · Simulation: ModelSim (Mentor Graphics), Incisive Enterprise Simulator – IES (Cadence)
  · Formal Verification (Cadence Incisive and Conformal Suite for Assertions)
- VHDL/Verilog Logic Synthesis & Optimization (Design Compiler/Synopsys, PrimeTime/Synopsys, RTL Compiler/Cadence)
- Design for Test, Test Pattern Generation (Synopsys DFT Compiler, Cadence RTL Compiler and Encounter Test)
- Place & Route (Cadence Encounter Digital Implementation System), OA views of digital libraries are available for MS-implementation flow
- Power Analysis (Cadence EPS and Voltus)
- Static Timing Analysis (Cadence Tempus, Synopsys PrimeTime)
- Digital CMOS libraries and IO Cells for 0.25 µm CMOS and 0.13 µm CMOS

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02/2016

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Prototyping Service

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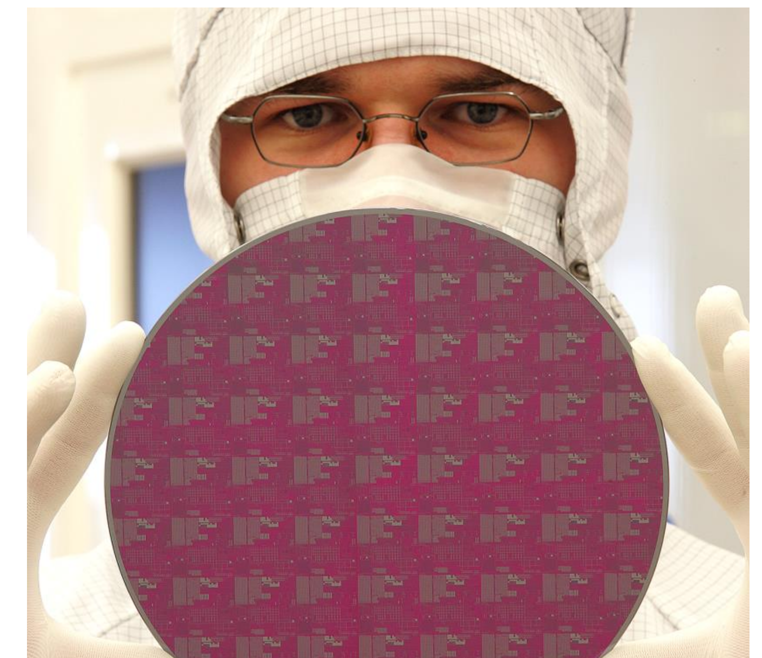

IHP is a German R & D institution, focused on wireless and broadband communication.
Core competencies are:

- Mixed signal process technology
- RF & digital circuit design
- Communication System Design

IHP is running an 8" pilot line housed in a 1.000-square-meter class-1 cleanroom.
Several 0.25 µm and 0.13 µm SiGe:C BiCMOS technologies are available